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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,261	06/25/2003	Ming-Shuoh Liang	N1085-00040 [TSMC2002-082	2865

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,261	LIANG ET AL.	
	Examiner	Art Unit	
	Matthew E Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-19,22 and 23* is/are rejected.

7)☒ Claim(s) *11,12,20,21,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings (particularly 3A-6B) do not clearly show the invention. The figures of the drawings seem to be photographs of such poor quality that it is hard to distinguish the structural elements. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Figures 1-2b should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13, which depend on claim 9, recites the limitations of "the outer rectilinear portion," and "the sawtooth pattern." There is insufficient antecedent basis for these limitations in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5, 8, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (US 6,100,589).

In re claim 1, Tanaka discloses (col. 6, line 20 – col. 7, line 38 and col. 9, line 2-23, and figs. 3, 7A-7B) a method of providing via for a multilayer semiconductor device, comprising: providing a first via set (112b) on a first layer (160) of a semiconductor device, further comprising: providing a substantially rectilinear first peripheral border on (500) a first layer of a semiconductor device, an interior of the first peripheral border

defining an inner area; providing a plurality of first via (112b) on the first layer of the semiconductor device within the inner area, the plurality of first via arranged in substantially parallel lines having a predetermined width, each of the plurality of first via having a predetermined separation distance to an adjacent first via; and providing a second via set (112a) on a second layer (150) of a semiconductor device, the second layer disposed above the first layer, the second layer further comprising: providing the second via set to be substantially identical to the first via set, the second via set disposed substantially parallel to the first via set in a plane defined by the second layer; and providing a conductive pathway (200) between a predetermined number of the first via of the first via set and those via of the second via set which are disposed substantially parallel to and substantially above the first via of the first via set.

In re claim 5, Tanaka shows (fig. 3, 7A and 7B) a multilayer semiconductor device, comprising: a first via set (112b) on a first layer (160) of a semiconductor device, further comprising: a substantially rectilinear first peripheral border (500) on a first layer of a semiconductor device, an interior of the first peripheral border defining an inner area; a plurality of first via (112b) on the first layer of a semiconductor device within the inner area, the plurality of first via arranged in substantially parallel lines having a predetermined width, each of the plurality of first via having a predetermined separation distance to an adjacent first via; and a second via set (112a) on a second layer (150) of a semiconductor device, the second layer disposed above the first layer, the second via set further comprising: a second via set substantially identical to the first via set, the

second via set disposed substantially parallel to the first via set in a plane defined by the second layer; and a conductive pathway between each of the first via of the first via set and each of the first via of the second via set disposed substantially parallel to and substantially above the first via of the first via set; and a pad (100) disposed at a surface of the semiconductor device; and a conductive pathway (200) operatively in communication with at least one of the first via of the first via set and the pad.

In re claims 8 and 15, Tanaka discloses (col. 6, line 20 – col. 7, line 38 and col. 9, line 2-23, and figs. 3, 7A, and 7B) a method of providing via for a multilayer semiconductor device and the semiconductor device, comprising: providing a first via set (112b) on a first layer (160) of a semiconductor device, further comprising: providing a first peripheral border (500 left) on a first layer of a semiconductor device; providing a second peripheral border (500 right) on the first layer, the second peripheral border disposed substantially parallel to the first peripheral border at a predetermined distance, the first peripheral border and the second peripheral border defining an inner area in between the first peripheral border and the second peripheral border; and providing a plurality of via (112b) on the first layer of a semiconductor device within the inner area, the first via arranged in substantially parallel lines having a predetermined width and a predetermined separation distance to an adjacent first via, the first via disposed substantially perpendicular to the first peripheral border and the second peripheral border; and providing a second via set (112a) on a second layer (150) of a semiconductor device, the second layer disposed above the first layer, further

comprising: providing a second via set (112a) substantially identical to the first via set, the second via set disposed substantially parallel to the first via set in a plane defined by the second layer; providing a conductive pathway (506) between the first peripheral border of the first via set and the first peripheral border of the second via set; providing a conductive pathway (506 right) between the second peripheral border of the first via set and the second peripheral border of the second via set; and providing a conductive pathway (200) between each of the first via of the first via set and each of the first via of the second via set disposed substantially parallel to and substantially above the first via of the first via set.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 6, 7, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (US 6,100,589) as applied to claims 1, 5, and 8 above, and further in view of the cited case law.

In re claims 2-4, 6, 7, and 14 Tanaka discloses the method wherein each substantially rectilinear first peripheral border is at least one of a rectangle. In re the rest of the limitations of the claims concerning the specific parameters such as separation distance, Tanaka does not specifically teach the desired distances and widths.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the separation distance and predetermined width of a specific value, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 9-10, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (US 6,100,589) as applied to claims 1 and 5 above, and further in view of Chen et al. (US 5,874,356).

In re claims 9, 10, 16, and 17, Tanaka shows all of the elements of the claims except the method of providing and the device having the peripheral borders with a repeating inner design, the design being a sawtooth pattern. Chen et al. shows (fig. 3) contact pad structure having a zig-zag (sawtooth) pattern formed in the inner peripheral border of the pad openings. With this configuration, stress is reduce in the opening thus forming a reliable bond (col. 3, lines 10-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the peripheral borders of Tanaka by forming a repeating sawtooth pattern as taught by Chen to reduce stress in the contact area and ultimately form a reliable bond.

Claims 18, 19, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (US 6,100,589) in view of Watanabe (US Pub 2003/0047794 A1).

In re claims 18 and 22, Tanaka discloses (col. 6, line 20 – col. 7, line 38 and col. 9, line 2-23, and figs. 3, 7A, and 7B) a method of providing via for a multilayer semiconductor device and the semiconductor device, comprising: providing a first via set (112b) on a first layer (160) of a semiconductor device, further comprising: providing a first peripheral border (500 left) on a first layer of a semiconductor device; providing a second peripheral border (500 right) on the first layer, the second peripheral border disposed substantially parallel to the first peripheral border at a predetermined distance, the first peripheral border and the second peripheral border defining an inner area in between the first peripheral border and the second peripheral border; and providing a plurality of via (112b) on the first layer of a semiconductor device within the inner area, the first via arranged in substantially parallel lines having a predetermined width and a predetermined separation distance to an adjacent first via, the first via disposed substantially perpendicular to the first peripheral border and the second peripheral border; and providing a second via set (112a) on a second layer (150) of a semiconductor device, the second layer disposed above the first layer, further comprising: providing a second via set (112a) substantially identical to the first via set, the second via set disposed substantially parallel to the first via set in a plane defined by the second layer; providing a conductive pathway (506) between the first peripheral border of the first via set and the first peripheral border of the second via set; providing

a conductive pathway (506 right) between the second peripheral border of the first via set and the second peripheral border of the second via set; and providing a conductive pathway (200) between each of the first via of the first via set and each of the first via of the second via set disposed substantially parallel to and substantially above the first via of the first via set. Tanaka shows all of the elements of the claims except the method of providing the device having the first, second, third, and fourth inner borders. It would have been obvious to one of ordinary skill in the art to use three, four, etc., borders since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).* See also MPEP 2144.04 VI. (B). However, Watanabe discloses [0106-1017] a method of providing a via and showing (fig. 13) a via set having first, second, third, and forth inner borders (21a) for suppressing erosion and dishing. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the via structure of Watanabe by forming multiple inner borders as taught by Watanabe to suppress erosion and dishing of the structure.

Allowable Subject Matter

Claims 11, 12, 20, 21, 24, and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
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September 19, 2004

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